

PART NUMBER

BOCOMI

CSMRLVGXXT8

COMPONENT SPECIFICATION

ISSUE 2

Component Specification For Hermetically Sealed, Radiation-Hard Latching Solid State Relay

Features	Applications
 Low on-state resistance 	■ Designed for 10 to 50V _{DC} Bus Application
 Selection of Operating Current and Voltage 	 Space Systems/Satellites
 SPST, SPDT, DPST, DPDT 	Space Battery Management Systems
 Full Military temperature range -55°C - +125°C 	Bus Control
 Military and Space Screening 	 Aerospace Power Distribution
■ Compatible with µC Drive	Power Isolation and Control
Internally IsolatedOutput Currents up to 3A	

DESCRIPTION

ISOCOM Latching Solid State Relays are designed to replace existing electro-mechanical relays (EMR). The CSMRLVGXXT8 is available in the single pole single throw (SPST), single pole double throw (SPDT), double pole single throw (DPST) and double pole double throw (DPDT) configuration. They are resilient to damage from shock and immune to contact-related problems (arcing, contamination) that are associated with mechanical equivalents. They are also lightweight in comparison to the EMR. Coupling between the input, output and power bus stages offers an effective isolation up to 500V. The latch and reset input stages are designed to directly interface with standard microcontrollers (μ C), requiring low current (< 10mA) with 3.3V or 5V logic. This device offers various operating voltage ranges from 10 to 50V with current capabilities up to 3A. Furthermore, it is featured in a 12 Pin TO-8 Package where each pin is isolated with a glass seal. This hermetic ceramic package comes with a gold plate finish and solder dip options available.









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STANDARDS

The following specifications have been complied with in the manufacturing of this product -

Aerospace Compliance Standards

AS9100D & ISO 9001:2015 - Design & Manufacture of Electronic and Optoelectronic Components (Ref GB15/92780)

Military Compliance Specifications

MIL-PRF-28750 - General Specification for Solid State Relay

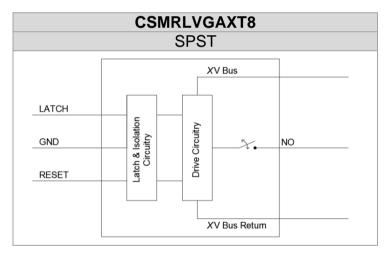
Military Compliance Standards

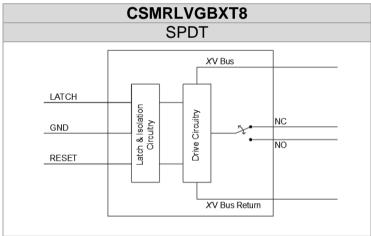
MIL-STD-883 - Test Method Standard Microcircuits

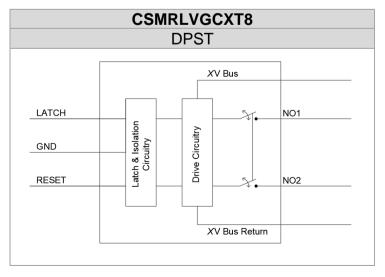
SCREENING INFORMATION

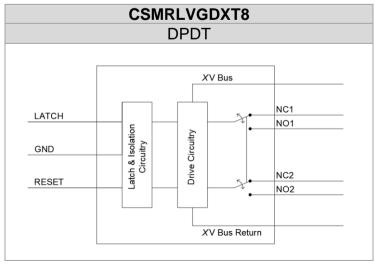
Our LSSR range can be screened to MIL-PRF-28750, applying test methods from MIL-STD-883. Please contact us for more information relating to the applicable screening processes.

FUNCTIONAL DIAGRAMS









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ABSOLUTE MAXIMUM RATINGS

 $T_A = 25$ °C U.O.S

Storage Temperature	-65° to +150°C
Operating Temperature	-55° to +125°C
Soldering Temperature	260°C
Continuous Output Current per relay – lo	See Selection Guide *
Output Voltage- Vo	See Selection Guide +10%
VLATCH	7V
Vreset	7V
Ісатсн	15mA
IRESET	15mA
Input-to-Output Isolation Voltage	爺500 V _{DC}
<i>X</i> VBus	50V

^{*}Current Limited by Package

ELECTRICAL CHARACTERISTICS

 $T_A = -55^{\circ}C$ to $+125^{\circ}C$ U.O.S

Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
		Input				
Latch voltage	V _{Latch}	$I_{Latch} = 10mA$	3	5		V
Reset voltage	V _{Rst}	$I_{Rst} = 10mA$	3	5		V
Latch Current	Latch	$V_{Latch} = 5V$	7	10	_	mA
Reset Current	I _{Rst}	$V_{Rst} = 5V$	'	10		ША
Latch/Reset reverse	B _{VR(Latch)}	$I_R = 10 \mu A$	5	_	_	V
breakdown voltage	B _{VR(Rst)}	<u> </u>	3			V
Latch pulse duration	PW _{Latch}	$V_{Latch} = 5V$	40	-	-	μs
Reset pulse duration	PW _{Rst}	$V_{Rst} = 5V$	40	-	-	μs
		Output				
	Bus (Latched)	X = 10V TO 50V,	_	8	_	mA
XVBus current	Tous (Laterieu)	mode = Latch				111/1
XVBus ourrent	I _{Bus(Unlatched)}	X = 10V TO 50V,	_	1.5	_	mA
		mode = Reset		1.0		
Output current	lo		See s	election of	nuide	Α
Output on state	R _(On))/ /01/TO TO!	(Page 7)		J 4.1 4. 5	mΩ
resistance (per output)	1 1(011)	X = 10V TO 50V		(3 - /		
Output leakage	loL		_	5	70	μA
Current		O a series d				' '
	I I	Coupled				
Input-to-output		I_{I-O} in to out = $1\mu A$,			F00	
isolation breakdown voltage (1)	V _{I-O}	$T_A = 25^{\circ}C$	-	-	500	V
Latch time (NO Latch)						
	T _{PL(NO)}		-	950	-	
Latch time (NC Latch)						-
(2)	T _{PL(NC)}	X = 10V TO 50V	-	150	-	
Reset latch delay (NO		I_{OX} = See selection guide				μs
to reset) (2)	T _{PR(NO)}	.o, coo concollon guido	-	250	-	
Reset latch delay (NC	_			1-0		-
to reset) (2)	T _{PR(NC)}		-	150	-	

Notes:

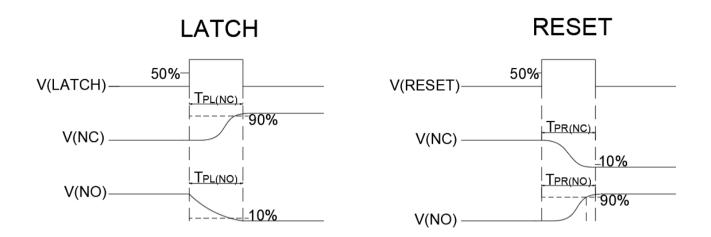
- (1) Inputs shorted together; outputs shorted together
- (2) See propagation timing delay measurements
- (3) For data on SOA please contact sales at ISOCOM Ltd

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PROPAGATION TIMING DELAY MEASUREMENTS



Switching Characteristics (Note: All Signals Measured with Respect to XV Bus Return)

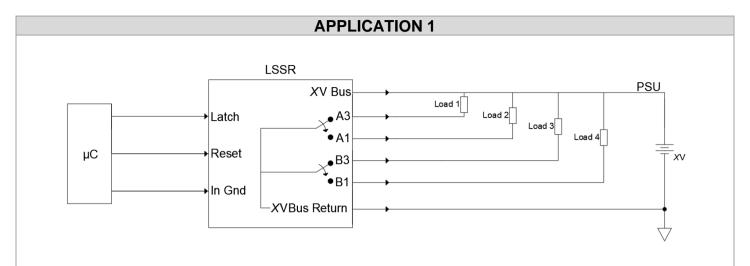
TRUTH TABLE

Bus Voltage	on	on	on	on	on	on	off	on
Latch	0	1	0	0	0	1	X	0
Reset	0	0	0	1	0	0	Х	0
NO status	Open	Closed	Closed	Open	Open	Closed	Open	Open
NC status	Closed	Open	Open	Closed	Closed	Open	Open	Closed

On initial powerup the LSSR is in its default condition. The normally open (NO) and normally closed (NC) outputs are open and closed respectively. Upon receiving a short input pulse to the LATCH input, the NO and NC terminals become closed and open circuit respectively. The device will then remain in the latched condition indefinitely or until a short input pulse to the RESET returns the outputs to their default conditions. Additionally, if the XV bus line is off while the LSSR is in the LATCH state, the device outputs automatically return to their default conditions upon the power reinstatement.

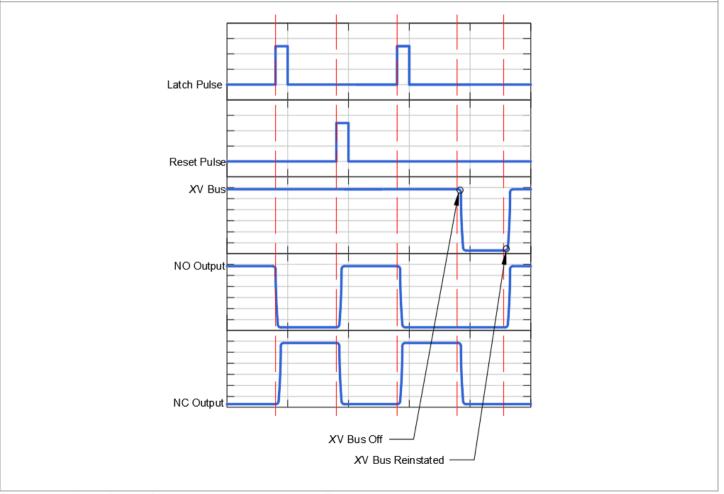


APPLICATIONS



Notes:

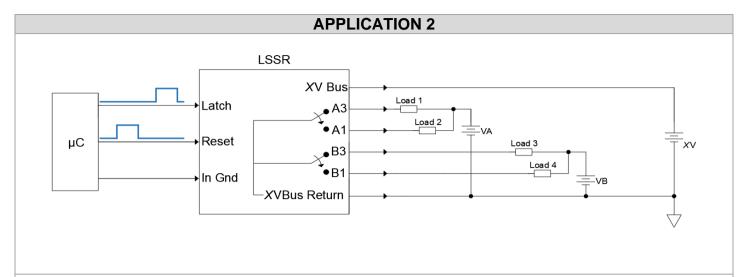
- For low side switching
- All loads connected to XV
- XV Bus Return has the sum of current from all loads and XV PSU
- Waveforms below measured at points A1/B1 (NO) and A3/B3 (NC) outputs with respect to XVBus Return



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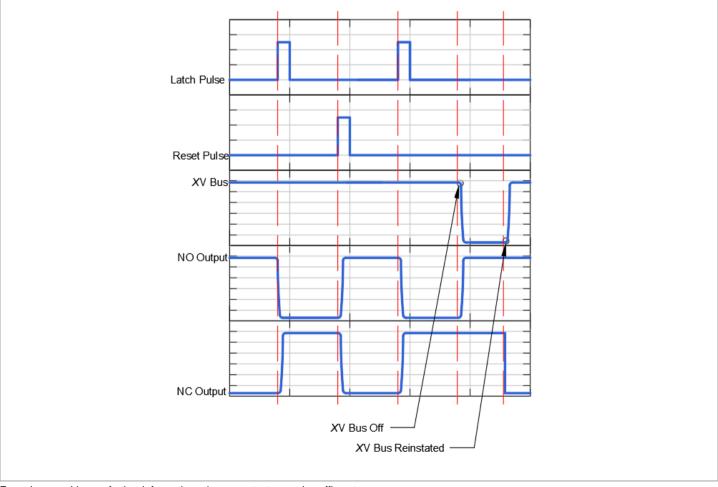
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Notes:

- For low side switching
- Can have an XV power supply for a virtual Vcc
- VA and VB can be independent supplies (and lower than XV)
- Can also be expanded to independent PSUs on the loads of A3, A1, B3 and B1
- All output supplies must share the same ground
- XV Bus Return has the sum of currents from VA, VB and XV
- Waveforms below measured at points A1/B1 (NO) and A3/B3 (NC) outputs with respect to XVBus Return



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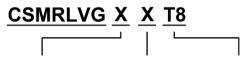
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SELECTION GUIDE

Bus Voltage (V)	I _D (A)	R _(ON) (TYP) (mΩ)
10-50	1	120

ORDERING PARTS



Part Reference	Circuit	Current (A)	Package Type
CSMRLVGXXT8	A (SPST) B (SPDT) C (DPST) D (DPDT)	1 3	TO-8

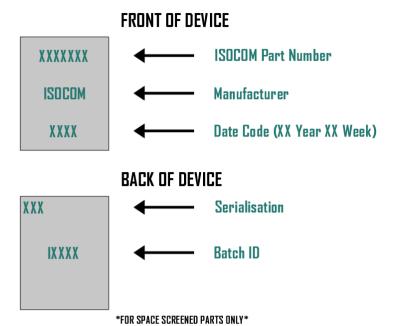
PACKAGE STYLES AND CONFIGURATION OPTIONS

Package	TO-8			
Lead Style	-			
Channels	Optional			
Common Channel Wiring	-			
ISOCOM Part Number and Options				
Commercial	CSMRLVGXXT8			
Defense Screen Level	CSMRLVGXXT8/L2			
Space Screen Level	CSMRLVGXXT8/L2S			
Standard Gold Plate Finish	Gold Plate			
Solder Dipped	Option #20			

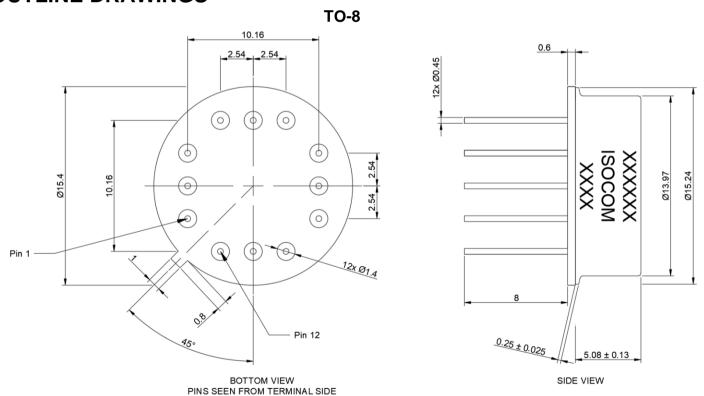
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DEVICE MARKING



OUTLINE DRAWINGS



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PIN OUT INFORMATION

Pin Number	Pin Function						
	SPST	SPDT	DPST	DPDT			
1	<i>X</i> VBus	<i>X</i> VBus	<i>X</i> VBus	<i>X</i> VBus			
2	XVBus Return	XVBus Return	XVBus Return	XVBus Return			
3	XVBus Return	XVBus Return	XVBus Return	XVBus Return			
4	-	NC1	-	NC1			
5	NO1	NO1	NO1	NO1			
6	XVBus Return	XVBus Return	XVBus Return	XVBus Return			
7	-	-	-	NO2			
8	-	-	NC2	NC2			
9	XVBus Return	XVBus Return	XVBus Return	XVBus Return			
10	Reset	Reset	Reset	Reset			
11	GND	GND	GND	GND			
12	Set	Set	Set	Set			

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aerospace sector certification scheme



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